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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
GOUDREAU, GEORGE A	

ART UNIT	PAPER NUMBER
1763	

DATE MAILED: 06/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/723,714	JI ET AL.	
	Examiner	Art Unit	
	George A. Goudreau	1763	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *(11-26-03' to 4-13-04')*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

George A Goudreau

GEORGE GOUDREAU
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 24-26, and 28-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Moise et. al. (6,211,035).

Moise et. al. disclose a process for anisotropically rie etching a PZT (i.e.-lead zirconium titanate) layer on the surface of a substrate (i.e.-a laminate) using a patterned SiO2 etch mask, and a plasma etchant, which is comprised of (CF4-Cl2-Ar). O2 may optionally be added to the plasma etchant. They further teach the equivalence in using other sources of chlorine in their plasma etchant such as BCl3. Also, they teach that other sources of oxygen such as CO may be used in their plasma etchant. This is discussed in columns 1-26. This is shown in figures 1-15.

3. Claims 24, and 26-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Kanniainen et. al. (1998').

Kanniainen et. al. disclose a process for rie etching a Ta2O5/HfO2 laminate structure on a semiconductor wafer using a plasma, which is comprised of BCl3-Cl2. This is discussed in the abstract.

4. Claims 24, and 26-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Nallan et. al. (2003/0170986).

Nallan et. al. disclose a process for rie etching a HfO2 layer (302) on the surface of a wafer (314) using a patterned photo resist etch mask (308), and a plasma, which is comprised of (Cl2-CO). This is discussed on pages 1-4. This is shown in figures 1-4.

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 1-2, 4-5, 8-9, 11-15, 17,19-23, and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moise et. al. as applied in paragraph 2 above.

Moise et. al. as applied in paragraph 2 above fail to specifically disclose the following aspects of applicant's claimed invention:

-the specific usage of an ADL (i.e.-atomic deposition process/ reactor) to form the PZT layer in the process taught above;

-the specific usage of the plasma etchant taught above to clean an ADL reactor, which has been used to deposit the PZT layer onto the surface of a substrate; and

-the specific plasma etching process condition, which are claimed by the applicant

It would have been obvious to one skilled in the art to use an ADL process/ reactor to form the PZT layer in the process taught above based upon the following. The usage of an ADL process/ reactor to form a metal oxide layer such as a PZT layer is conventional or at least well known in the semiconductor processing arts. (The examiner takes official notice in this regard.) Further, this simply represents the usage of an alternative, and at least equivalent means for forming the PZT layer in the process taught above to the specific usage of other such means.

It would have been obvious to one skilled in the art to use the plasma etchant taught above to clean an ADL reactor used to form a PZT layer onto the surface of a substrate between process runs based upon the following. The usage of a plasma cleaning process to clean the interior surfaces of a reactor used to coat a semiconductor substrate is conventional or at least well known in the semiconductor processing arts. (The examiner takes official notice in this regard.) Also, it is desirable to reduce the amount of contamination of the surface of a substrate, which is processed through a coating process between successive process runs by removing any film,

which forms on the interior surfaces of the coater during the coating process. (Such films can undesirably flake off the interior walls of the reactor, and fall onto the surface of a substrate to be coated in a subsequent process run. Such flake material then acts as a source of contamination of the surface of the substrate to be coated.) Further, Moise et. al. teach that their plasma etching process provides a desirable means for removing a PZT layer from the surface of a substrate.

It would have been prima facie obvious to employ any of a variety of different process parameters in the etching process taught above including those which are specifically claimed by the applicant. These are all well known variables in the plasma etching art, which are known to effect both the rate and the quality of the plasma etching process. Further, the selection of particular values for these variables would not necessitate any undo experimentation, which would have been indicative of unexpected results.

Alternatively, it would have been obvious to one skilled in the art to employ the specific etch process parameters which are claimed by the applicant based upon In re Aller as cited below.

"Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F. 2d 454, 105 USPQ 233, 235 (CCPA).

Further, all of the specific process parameters, which are claimed by the applicant are results effective variables whose values are known to effect both the rate, and the quality of the plasma etching process.

8. Claims 24-26, and 28-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ingrey et. al. (4,030,967).

Ingrey et. al. disclose a process for plasma etching an Al2O3 layer on the surface of an Al wiring layer (i.e.- a laminate) on top of a semiconductor substrate using a patterned photo resist etch mask, and a plasma comprised of BCl3. This is discussed in columns 1-4. This is shown in figures 1-2. Ingrey et. al. fail, however, to specifically disclose the following aspects of applicant's claimed invention:

-the specific etch process parameters which are claimed by the applicant; and

-the specific usage of an inert gas in the plasma etchant

It would have been obvious to one skilled in the art to use an inert gas as a diluent in the plasma etchant taught above based upon the following. The usage of an inert gas as a diluent in a plasma etchant is conventional or at least well known in the plasma etching arts. (The examiner takes official notice in this regard.) Further, this would simply represent the usage of an alternative, and at least equivalent means for conducting the etching process taught above to the specific means, which are taught above.

It would have been prima facie obvious to employ any of a variety of different process parameters in the etching process taught above including those which are specifically claimed by the applicant. These are all well known variables in the plasma etching art, which are known to effect both the rate and the quality of the plasma etching process. Further, the selection of particular values for these variables would not

necessitate any undo experimentation, which would have been indicative of unexpected results.

Alternatively, it would have been obvious to one skilled in the art to employ the specific etch process parameters which are claimed by the applicant based upon In re Aller as cited above. Further, all of the specific process parameters, which are claimed by the applicant are results effective variables whose values are known to effect both the rate, and the quality of the plasma etching process.

9. Claims 1-5, 8-9, 13-15, 17, 19-21, 24, and 26-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pomarede et. al. (6,613,695) further in view of Nallan et. al. (2003/0170986).

Pomarede et. al. disclose a process for depositing a gate dielectric (i.e.-a laminate) onto the surface of wafer using an ALD process. The gate dielectric may be any of Al2O3, HfO2, ZrO2, Ta2O5, BST, or SBT. This is discussed in columns 1-18. Pomarede et. al. fail, however, to specifically disclose the following aspects of applicant's claimed invention:

-the specific etch process parameters, which are claimed by the applicant;

-the specific etching of the HfO2 gate layer on the wafer using a plasma comprised of (Cl2-CO);

-the specific cleaning of the ALD reactor which was used to deposit the HfO2 layer onto the surface of the wafer after a targeted number of process runs using a plasma comprised of (Cl2-CO); and

-the specific usage of an inert gas in the plasma etchant used to etch the HfO2 layer

Nallan et. al. teach that it is desirable to etch a HfO2 layer on a wafer using plasma, which is comprised of (Cl2-CO). This is discussed on pages 1-4. This is shown in figures 1-4.

It would have been obvious to one skilled in the art to pattern the HfO2 gate layer in the process taught above using a plasma comprised of (Cl2-CO) based upon the following. It is conventional or at least well known in the semiconductor arts to pattern a gate dielectric layer using a plasma etching process. (The examiner takes official notice in this regard.) The specific usage of the plasma etching method taught by Nallan et. al. to pattern the gate layer in the process taught above simply represents the usage of an alternative, and at least equivalent means for patterning the gate dielectric to the specific usage of other such means for doing so. Further, Nallan et. al. teach that it is desirable to etch a HfO2 layer on a wafer using a plasma, which is comprised of (Cl2-CO).

It would have been obvious to one skilled in the art to use the plasma etchant taught above to clean an ADL reactor used to form a HfO2 layer onto the surface of a substrate between process runs based upon the following. The usage of a plasma cleaning process to clean the interior surfaces of a reactor used to coat a semiconductor substrate is conventional or at least well known in the semiconductor processing arts. (The examiner takes official notice in this regard.) Also, it is desirable to reduce the amount of contamination of the surface of a substrate, which is processed

through a coating process between successive process runs by removing any film, which forms on the interior surfaces of the coater during the coating process. (Such films can undesirably flake off the interior walls of the reactor, and fall onto the surface of a substrate to be coated in a subsequent process run. Such flake material then acts as a source of contamination of the surface of the substrate to be coated.) Further, Nallan et. al. teach that their plasma etching process provides a desirable means for etching an HfO2 layer on the surface of a wafer.

It would have been obvious to one skilled in the art to use an inert gas as a diluent in the plasma etchant taught above based upon the following. The usage of an inert gas as a diluent in a plasma etchant is conventional or at least well known in the plasma etching arts. (The examiner takes official notice in this regard.) Further, this would simply represent the usage of an alternative, and at least equivalent means for conducting the etching process taught above to the specific means, which are taught above.

It would have been prima facie obvious to employ any of a variety of different process parameters in the etching process taught above including those which are specifically claimed by the applicant. These are all well known variables in the plasma etching art, which are known to effect both the rate and the quality of the plasma etching process. Further, the selection of particular values for these variables would not necessitate any undo experimentation, which would have been indicative of unexpected results.

Alternatively, it would have been obvious to one skilled in the art to employ the specific etch process parameters which are claimed by the applicant based upon In re Aller as cited above. Further, all of the specific process parameters, which are claimed by the applicant are results effective variables whose values are known to effect both the rate, and the quality of the plasma etching process.

10. Claims 1-4, 6, 8, 10, 13-14, 16-17, 19-21, and 24-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pomarede et. al. (6,613,695) further in view of Kanniainen et. al. (1998').

Pomarede et. al. disclose a process for depositing a gate dielectric onto the surface of wafer (i.e.-a laminate) using an ALD process. The gate dielectric may be any of Al2O3, HfO2, ZrO2, Ta2O5, BST, or SBT. This is discussed in columns 1-18. Pomarede et. al. fail, however, to specifically disclose the following aspects of applicant's claimed invention:

-the specific etch process parameters, which are claimed by the applicant;

-the specific etching of the HfO2 gate layer on the wafer using a plasma comprised of (BCl3-Cl2);

-the specific cleaning of the ALD reactor which was used to deposit the HfO2 layer onto the surface of the wafer after a targeted number of process runs using a plasma comprised of (BCl3-Cl2); and

-the specific usage of an inert gas in the plasma etchant used to etch the HfO2 layer

Kanniainen et. al. teach that it is desirable to etch a HfO2 layer on a wafer

using plasma, which is comprised of (BCl3-Cl2). This is discussed in the abstract.

It would have been obvious to one skilled in the art to pattern the HfO2 gate layer in the process taught above using a plasma comprised of (BCl3-Cl2) based upon the following. It is conventional or at least well known in the semiconductor arts to pattern a gate dielectric layer using a plasma etching process. (The examiner takes official notice in this regard.) The specific usage of the plasma etching method taught by Kanniainen et. al. to pattern the gate layer in the process taught above simply represents the usage of an alternative, and at least equivalent means for patterning the gate dielectric to the specific usage of other such means for doing so. Further, Kanniainen et. al. teach that it is desirable to etch a HfO2 layer on a wafer using a plasma, which is comprised of (BCl3-Cl2).

It would have been obvious to one skilled in the art to use the plasma etchant taught above to clean an ADL reactor used to form a HfO2 layer onto the surface of a substrate between process runs based upon the following. The usage of a plasma cleaning process to clean the interior surfaces of a reactor used to coat a semiconductor substrate is conventional or at least well known in the semiconductor processing arts. (The examiner takes official notice in this regard.) Also, it is desirable to reduce the amount of contamination of the surface of a substrate, which is processed through a coating process between successive process runs by removing any film, which forms on the interior surfaces of the coater during the coating process. (Such films can undesirably flake off the interior walls of the reactor, and fall onto the surface of a substrate to be coated in a subsequent process run. Such flake material then acts

as a source of contamination of the surface of the substrate to be coated.) Further, Kanniainen et. al. teach that their plasma etching process provides a desirable means for etching an HfO2 layer on the surface of a wafer.

It would have been obvious to one skilled in the art to use an inert gas as a diluent in the plasma etchant taught above based upon the following. The usage of an inert gas as a diluent in a plasma etchant is conventional or at least well known in the plasma etching arts. (The examiner takes official notice in this regard.) Further, this would simply represent the usage of an alternative, and at least equivalent means for conducting the etching process taught above to the specific means, which are taught above.

It would have been prima facie obvious to employ any of a variety of different process parameters in the etching process taught above including those which are specifically claimed by the applicant. These are all well known variables in the plasma etching art, which are known to effect both the rate and the quality of the plasma etching process. Further, the selection of particular values for these variables would not necessitate any undo experimentation, which would have been indicative of unexpected results.

Alternatively, it would have been obvious to one skilled in the art to employ the specific etch process parameters which are claimed by the applicant based upon In re Aller as cited above. Further, all of the specific process parameters, which are claimed by the applicant are results effective variables whose values are known to effect both the rate, and the quality of the plasma etching process.

11. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

12. Claims 1-10, 13-21, and 24-30 are provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1-26 of copending Application No. 10/410,803. This is a provisional double patenting rejection since the conflicting claims have not in fact been patented.

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

14. Any inquiry concerning this communication should be directed to examiner George A. Goudreau at telephone number 571-272-1434.

George A. Goudreau
Primary Examiner
Art Unit 1763